

Liverpool John Moores University

Title: Microprocessors and Software
Status: Definitive
Code: **4606IYO** (124218)
Version Start Date: 01-08-2021

Owning School/Faculty: Engineering
Teaching School/Faculty: Study Group

| Team | Leader |
|--------------|--------|
| Michael Shaw | Y |
| Jack Mullett | |

Academic Level: FHEQ4 **Credit Value:** 10 **Total Delivered Hours:** 47
Total Learning Hours: 100 **Private Study:** 53

Delivery Options

Course typically offered: Semester 2 and Summer

| Component | Contact Hours |
|-----------|---------------|
| Lecture | 30 |
| Practical | 15 |

Grading Basis: 40 %

Assessment Details

| Category | Short Description | Description | Weighting (%) | Exam Duration |
|----------|-------------------|-----------------------|---------------|---------------|
| Exam | Exam | Invigilated exam/test | 100 | 2 |

Aims

Provide an overview of the operation of modern microprocessors/microcontrollers and the mechanisms used to represent and process information. Design and implement applications written in both low level and high level languages.

Learning Outcomes

After completing the module the student should be able to:

- 1 Describe the techniques applied to represent information within a Microprocessor. Describe the instruction set of a computer contrasting RISC and CISC approaches.
- 2 Identify the fundamental components of a Microprocessor. Demonstrate an understanding of the registers that constitute a Microprocessor.
- 3 Describe the role of modern Operating Systems in embedded, mobile, desktop and server environments.
- 4 Specify and design microprocessor applications, then implement them utilising high or low level languages

Learning Outcomes of Assessments

The assessment item list is assessed via the learning outcomes listed:

| | | | | |
|-----------|---|---|---|---|
| Exam/test | 1 | 2 | 4 | 3 |
|-----------|---|---|---|---|

Outline Syllabus

Binary, HEX, 2s Complement, Number endianness, IEEE 754, ASCII, UNICODE.

Processor core and cache hierarchies, Buses, Memory Organisation, Cache Coherency, Multicore, 80% 20% ratio.

Application Scheduling, Security, Interrupt Handling, Libraries, Communications. Variables, Arrays, Iteration, Selection, Interaction with I/O, Structures, Flow charts.

Learning Activities

Lecture, demonstration and practical activities applying topics discussed.

Notes

This module introduces the fundamentals of Computer architecture and the development of High level software.