LIVERPOOL JOHN MOORES UNIVERSITY

Digital System Design

Module Information

2022.01, Approved

Summary Information

Module Code	5503ICBTEL
Formal Module Title	Digital System Design
Owning School	Engineering
Career	Undergraduate
Credits	15
Academic level	FHEQ Level 5
Grading Schema	40

Teaching Responsibility

LJMU Schools involved in Delivery
LJMU Partner Taught

Partner Teaching Institution

Institution Name
International College of Business and Technology

Learning Methods

Learning Method Type	Hours
Lecture	45
Tutorial	10
Workshop	5

Module Offering(s)

Display Name	Location	Start Month	Duration Number Duration Unit
APR-PAR	PAR	April	12 Weeks

JAN-PAR	PAR	January	12 Weeks
SEP_NS-PAR	PAR	September (Non-standard start date)	12 Weeks

Aims and Outcomes

Aims	This module introduce and develop a comprehensive understanding of the principles, procedures and applications of Digital System design based on PLDs and FPGAs.

After completing the module the student should be able to:

Learning Outcomes

Code	Number	Description
MLO1	1	Explain the top-down design process through the levels of abstraction from high-level system description down to gate-level and transistor level implementation.
MLO2	2	Apply various styles (behavioural, structural and physical) to describe the digital system in the hardware description language systems.
MLO3	3	Build behavioural and synthesis of Verilog-HDL descriptions of basic components and digital systems include combinational and sequential logic circuits and predict the behaviour of a digital system or the simulation result of a Verilog-HDL code.
MLO4	4	Apply Electronic Design Automation (EDA) tools and Hardware Description Languages to design and synthesize digital system(s) and apply on-chip debugging techniques for modern FPGA/CPLD-based hardware platforms such as Xilinx Spartan FPGA devices.

Module Content

Outline Syllabus	Digital system design process. EDA tools and design viewpoints. Behavioural, dataflow, and gate-level descriptions. Hardware description languages. VHDL modelling concepts. Behavioural and structural architecture descriptions. Concurrent and sequential statements. Event-driven simulation. Building blocks for digital systems: tri-state buffers, multiplexers, latches, flip-flops, registers, counters, arithmetic circuits, finite state machines. Design methodology. Synchronous systems. Top down design. Register-transfer-level design. Test benches. Synthesis from VHDL. Implementation issues: gate delays, timing, critical path, communication between unsynchronised machines, coping with metastability.Introduction to Programmable Logic Devices (FPGAs, CPLDs).
Module Overview	
Additional Information	

Assessments

Assignment Category	Assessment Name	Weight	Exam/Test Length (hours)	Module Learning Outcome Mapping
Report	Coursework	30	0	MLO1, MLO4
Exam	Exam	70	2	MLO2, MLO3

Module Contacts

Module Leader

Contact Name	Applies to all offerings	Offerings
Karl Jones	Yes	N/A

Partner Module Team

Contact Name	Applies to all offerings	Offerings