Liverpool John Moores University

Title:	DIGITAL SYSTEM DESIGN
Status:	Definitive
Code:	**5503ICBTEL** (127021)
Version Start Date:	01-08-2021
Owning School/Faculty:	Engineering
Teaching School/Faculty:	ICBT, Colombo

Team	Leader
Alison Cotgrave	Y

Academic Level:	FHEQ5	**Credit Value:**	15	**Total Delivered Hours:**	62
Total Learning Hours:	150	**Private Study:**	88		

Delivery Options
Course typically offered: S2 and Non Std S2 (S2 for Jan)

Component	Contact Hours
Lecture	45
Tutorial	10
Workshop	5

Grading Basis: 40 %

Assessment Details

Category	Short Description	Description	Weighting (%)	Exam Duration
Report	AS1	Coursework (1500 words)	30	
Exam	AS2	Exam	70	2

Aims

This module introduce and develop a comprehensive understanding of the principles, procedures and applications of Digital System design based on PLDs and FPGAs.

Learning Outcomes

After completing the module the student should be able to:

1 Explain the top-down design process through the levels of abstraction from high-level system description down to gate-level and transistor level implementation.
2 Apply various styles (behavioural, structural and physical) to describe the digital system in the hardware description language systems.
3 Build behavioural and synthesis of Verilog-HDL descriptions of basic components and digital systems include combinational and sequential logic circuits and predict the behaviour of a digital system or the simulation result of a Verilog-HDL code.
4 Apply Electronic Design Automation (EDA) tools and Hardware Description Languages to design and synthesize digital system(s) and apply on-chip debugging techniques for modern FPGA/CPLD-based hardware platforms such as Xilinx Spartan FPGA devices.

Learning Outcomes of Assessments

The assessment item list is assessed via the learning outcomes listed:

Coursework	1	4
Exam	2	3

Outline Syllabus

Digital system design process. EDA tools and design viewpoints. Behavioural, dataflow, and gate-level descriptions.

Hardware description languages. VHDL modelling concepts. Behavioural and structural architecture descriptions. Concurrent and sequential statements. Event-driven simulation.

Building blocks for digital systems: tri-state buffers, multiplexers, latches, flip-flops, registers, counters, arithmetic circuits, finite state machines.

Design methodology. Synchronous systems. Top down design. Register-transfer-level design. Test benches. Synthesis from VHDL.

Implementation issues: gate delays, timing, critical path, communication between unsynchronised machines, coping with metastability.

Introduction to Programmable Logic Devices (FPGAs, CPLDs).

Learning Activities

Students will be supported in their learning, to achieve the above learning outcomes, in the following ways:

Advanced digital theories acquire through lectures, seminars and tutorials, and

control system applications learn through case studies.

Digital design using PLD's and FPGA cover through the simulation laboratory and the practical.

Notes

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