Computer Architecture

Module Information

2022.01, Approved

Summary Information

Module Code	5614TECYPC
Formal Module Title	Computer Architecture
Owning School	Engineering
Career	Undergraduate
Credits	10
Academic level	FHEQ Level 5
Grading Schema	40

Teaching Responsibility

LJMU Schools involved in Delivery
LJMU Partner Taught

Partner Teaching Institution

Institution Name
YPC International College (Kolej Antarabangsa YPC)

Learning Methods

Learning Method Type	Hours
Lecture	24
Tutorial	18

Module Offering(s)

Display Name	Location	Start Month	Duration Number Duration Unit
JAN-PAR	PAR	January	12 Weeks

Aims and Outcomes

Aims	The aim of the module is to enable students to gain an understanding and overview of computer architecture at the hardware and software levels.

After completing the module the student should be able to:

Learning Outcomes

Code	Number	Description
MLO1	1	Understand the digital representation of data in a computer system
MLO2	2	State the operation and design of logic gates to use Boolean algebra in representing logic circuit
MLO3	3	Explain computer architecture in terms of processor, memory, bus, interconnection, machine instruction cycle and different I/O devices
MLO4	4	Explain principles of operating systems and their operation via processes, threads and scheduling

Module Content

Outline Syllabus	Data representation: Number system, binary numbers, addition, subtraction and complements.Logic circuits: The use of Boolean algebra to write equations that describe logic circuits and the basic techniques used to manipulate Boolean equations. The design and Construction of Logic circuits, both synchronous and asynchronous, including encoders, decoders and adders.Computer hardware: Processor design and operation, memory and file system, file allocation, Input/output devices and peripherals, bus architectures, fetch-execute cycle.Operating systems: The role of the operating system, resource management, processes, and threads, non-pre-emptive and pre-emptive scheduling.
Module Overview	
Additional Information	This module provides an overview of data representation, logic circuits, hardware and operating systems in computer architectures.

Assessments

Assignment Category	Assessment Name	Weight	Exam/Test Length (hours)	Module Learning Outcome Mapping
Exam	Examination	100	2	MLO1, MLO2, MLO3, MLO4

Module Contacts

Module Leader

Contact Name	Applies to all offerings	Offerings
Karl Jones	Yes	N/A

Partner Module Team

Contact Name	Applies to all offerings	Offerings