

## Liverpool John Moores University

Title: PROGRAMMABLE ELECTRONIC DEVICES  
Status: Definitive  
Code: **6016ENG** (106221)  
Version Start Date: 01-08-2016

Owning School/Faculty: Electronics and Electrical Engineering  
Teaching School/Faculty: Electronics and Electrical Engineering

Team	Leader
Michael Shaw	Y

**Academic Level:** FHEQ6      **Credit Value:** 12      **Total Delivered Hours:** 38  
**Total Learning Hours:** 120      **Private Study:** 82

### Delivery Options

Course typically offered: Standard Year Long

Component	Contact Hours
Lecture	12
Practical	18
Tutorial	6

**Grading Basis:** 40 %

### Assessment Details

Category	Short Description	Description	Weighting (%)	Exam Duration
Exam	AS1	Examination	50	2
Essay	AS2	Coursework	50	

### Aims

*This module aims to provide a comprehensive insight into the modern development of programmable electronic architectures. Students will gain a theoretical understanding of current and future trends, as well as practical experience of designing complex systems using Xilinx FPGA devices.*

## Learning Outcomes

After completing the module the student should be able to:

- 1 Propose the most appropriate modern design structures for particular applications.
- 2 Design using modern CPLD, FPGA and reconfigurable architectures.
- 3 Confidently use a proprietary CAD tool such as Xilinx, to design, test and fabricate a complex digital system.
- 4 Incorporate industry standard test methodologies into designs.

## Learning Outcomes of Assessments

The assessment item list is assessed via the learning outcomes listed:

EXAM	1	2	4	
CW	1	2	3	4

## Outline Syllabus

*Review of programmable architectures: PROM, PLD, EPLD, PAL, GAL, CLB, CPLD & FPGA. Design using reconfigurable systems. Combinational, synchronous and asynchronous sequential design in programmable logic. Considerations for high speed systems, metastability and clock distribution, transmission line considerations. Design, test, simulation and implementation using a proprietary CAD tool such as Xilinx. Design for testability and reliability, JTAG Boundary Scan (IEEE 1149.1), BIST methods, in-circuit testing, scan path method.*

## Learning Activities

By a combination of lectures, tutorials and laboratory design assignments.

## Notes

This level 3 module will provide undergraduates with a comprehensive understanding and develop a strong skill-set in industry-standard theoretical and practical knowledge for the design of modern programmable logic systems.