Liverpool John Moores University

Title:	FPGA
Status:	Definitive
Code:	**6501TECSBC** (113914)
Version Start Date:	01-08-2016
Owning School/Faculty:	Electronics and Electrical Engineering
Teaching School/Faculty:	The Sino-British College

Team	Leader
Colin Wright	Y

Academic Level:	FHEQ6	**Credit Value:**	12	**Total Delivered Hours:**	37
Total Learning Hours:	120	**Private Study:**	83		

Delivery Options
Course typically offered: Semester 2

Component	Contact Hours
Lecture	20
Practical	5
Tutorial	10

Grading Basis: 40 %

Assessment Details

Category	Short Description	Description	Weighting (%)	Exam Duration
Exam	AS1	Examination	70	2
Report	AS2	Coursework	30	

Aims

To acquire the skills required to implement digital hardware design in modern programmable logic devices, concentrating on mid range field programmable gate arrays (FPGA).

Learning Outcomes

After completing the module the student should be able to:

1 Perform a critical review of available programmable logic devices in order to select an appropriate technology for a particular problem.
2 nalyze a hardware design problem and individually produce a suitable design solution using a variety of methods – schematic capture, state machine design and hardware descriptor language
3 Apply their understanding of digital logic systems to devise a test bench to enable behavioral simulation of a circuit
4 Use the Xilinx ISE design tool set to synthesize a design, configure the target device and download the data file to the FPGA hardware

Learning Outcomes of Assessments

The assessment item list is assessed via the learning outcomes listed:

Exam	1	2	3
Report	2	3	4

Outline Syllabus

Design using reconfigurable systems. Combinational, synchronous and asynchronous sequential design in programmable logic. Considerations for high speed systems, metastability and clock distribution, transmission line considerations. Input and output options. Introduction to VHSIC Hardware Descriptor Language (VHDL) programming. Use of embedded microprocessors in FPGA designs. Design, test, simulation and implementation on a Xilinx Spartan 3E FPGA, using the proprietary CAD tool Xilinx ISE.

Learning Activities

By a combination of lectures, tutorials and laboratory design assignments.

Notes

This level 3 module will provide undergraduates with a comprehensive understanding and develop a strong skill-set in industry standard theoretical and practical knowledge for the design of modern programmable logic systems.