Liverpool John Moores University

Title:	PROGRAMMABLE ELECTRONIC DEVICES
Status:	Definitive
Code:	**6524ENGIOM** (117274)
Version Start Date:	01-08-2016
Owning School/Faculty:	Maritime and Mechanical Engineering
Teaching School/Faculty:	Maritime and Mechanical Engineering

Team	Leader
Russell English	Y
Colin Wright	

Academic Level:	FHEQ6	**Credit Value:**	20	**Total Delivered Hours:**	42
Total Learning Hours:	200	**Private Study:**	158		

Delivery Options
Course typically offered: Standard Year Long

Component	Contact Hours
Lecture	28
Practical	12
Tutorial	2

Grading Basis: 40 %

Assessment Details

Category	Short Description	Description	Weighting (%)	Exam Duration
Dissertation	Disser		100	

Aims

The aim of this module is to enhance the students' knowledge and understanding of the use of programmable electronic devices. In particular the use of Field Programmable Gate Array (FPGA) devices as an alternative to Application Specific Integrated Circuits (ASIC).

Learning Outcomes

After completing the module the student should be able to:

1	Apply knowledge of the internal architecture and characteristics of a typical field programmable gate array (FPGA) device to make decisions regarding architecture usage in an FPGA system design
2	Be able to interface external hardware to an FPGA device using techniques such as switch de-bouncing and display multiplexing.
3	Use a combination of schematic entry and hardware descriptor language (VHDL) to create the source files for the implementation of a modular system design using a proprietary software environment such as Xilinx ISE.
4	Design suitable test bench sources to test individual modules using one of the development software's simulation programs
5	Configure and test a design using a development board

Learning Outcomes of Assessments

The assessment item list is assessed via the learning outcomes listed:

Dissertation	1	2	3	4	5

Outline Syllabus

Review of programmable architectures: PROM, PLD, EPLD, PAL, CLB, CPLD & FPGA. Design using reconfigurable systems. Combinational, synchronous and asynchronous sequential design in programmable logic. Considerations for high speed systems, metastability and clock distribution, transmission line considerations. Introduction to the hardware descriptor language VHDL. State machine design using VHDL. Design, test, simulation and implementation using a proprietary CAD tool such as Xilinx. Design for testability and reliability, JTAG Boundary Scan (IEEE 1149.1), BIST methods, in-circuit testing, scan path method.

Learning Activities

By a combination of lectures and laboratory design assignments

Notes

This level 6 module will provide undergraduates with a comprehensive understanding and develop a strong skill-set in industry standard theoretical and practical knowledge for the design of modern programmable logic systems.