LIVERPOOL JOHN MOORES UNIVERSITY

VLSI Devices, Fabrication and Testing

Module Information

2022.01, Approved

Summary Information

Module Code	7305ELE
Formal Module Title	VLSI Devices, Fabrication and Testing
Owning School	Engineering
Career	Undergraduate
Credits	20
Academic level	FHEQ Level 7
Grading Schema	50

Teaching Responsibility

LJMU Schools involved in Delivery
Engineering

Learning Methods

Learning Method Type	Hours
Lecture	22
Practical	6
Tutorial	11

Module Offering(s)

Display Name	Location	Start Month	Duration Number Duration Unit
JAN-CTY	CTY	January	12 Weeks

Aims and Outcomes

Aims	To develop an understanding of the state-of-the-art CMOS devices and systems.To gain knowledge in the fabrication and testing of microelectronic devices.To enhance knowledge in latest consumer electronic products.

After completing the module the student should be able to:

Learning Outcomes

Code	Number	Description
MLO1	1	Show knowledge of the theory and problems of advanced microelectronic devices
MLO2	2	Appraise MOS fabrication process and techniques
MLO3	3	Evaluate testing techniques and appreciate reliability issues
MLO4	4	Model the device ageing process and use the model to predict device lifetime

Module Content

Outline Syllabus	An overview of the history of microelectronic industry and the milestones in thetheory of microelectronic devicesAdvanced microelectronic devices and systems: submicrometer MOSFETs,FINFETs, non-volatile memories, SOI transistors and thin film transistors (TFTs), andnano-wire devices. Liquid Crystal Display (LCD) systems and Charge-CoupledDevices (CCDs) cameras. Short-channel effects: charge sharing effects, draininduced barrier lowering and gate induced leakage current. New materials formetals, gate dielectrics, and semiconductors.Fabrications: typical MOS process flow and techniques, wafer cleaning, deposition(CVD and PECVD), masks and lithography, ion implantation, metallization, oxidation,epitaxy, dry etching (plasma and reactive ions), isolation techniques, and devicevariabilities.Testing and reliabilities: typical procedure and techniques, time-dependent dielectricbreakdown (TDDB) and stress-induced-leakage-currents (SILC), Fowler-Nordheiminjection, interface states and space charges in the oxide, the high and lowfrequency differential capacitance-voltage techniques, hot carrier induceddegradation, bias temperature instabilities, lifetime prediction.
Module Overview	
Additional Information	This level 7 module extends a prospective student's knowledge of the state-of-the-artelectronic devices and systems. The emphasis is on the differences between anadvanced device and a traditional one. The fabrication, testing and reliability issueswill be addressed.

Assessments

Assignment Category	Assessment Name	Weight	Exam/Test Length (hours)	Module Learning Outcome Mapping
Centralised Exam	Exam	70	2	MLO1, MLO2, MLO3
Report	Report	30	0	MLO1, MLO2, MLO4

Module Contacts

Module Leader

Contact Name	Applies to all offerings	Offerings
Jian Zhang	Yes	N/A

Partner Module Team

Contact Name	Applies to all offerings	Offerings